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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 10/805,158
Filing Date: March 19, 2004
Appellant(s): ONO ET AL.

Mr. Gerald Maliszewski, reg. No. 38,054
For Appellant

**EXAMINER'S ANSWER**



This is in response to the appeal brief filed on 11/20/2006 appealing from the Office action mailed 9/25/2006.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

No amendment after final has been filed.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

| | | |
|---|---|---|
| 20010015453 | AGARWAL | 8-2001 |
| 5372957 | LIANG | 12-1994 |
| 5846883 | MOSLEHI | 8-1998 |
| 6451641 | HALLIYAL | 9-2002 |
| 6486080 | CHOOI | 11-2002 |
| 6754104 | KING | 6-2004 |

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

**Claims 16, 17, 20-22, and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halliyal (US 6451641) in view of King (US 6754104) and Kirkpatrick (US 4197144).**

Regarding claim 16, Halliyal shows most aspects of the instant invention including a method of fabricating a non-volatile memory transistor comprising the steps of:

- ✓ Preparing a semiconductor substrate (see, *e.g.*, fig. 5/step S501)
- ✓ Forming a gate stack on the substrate as follows:
  - Depositing a single layer of high-k dielectric material, without an underlying oxide insulator layer and an overlying oxide insulator layer (see, *e.g.*, fig. 5/step S502)
  - Forming an electrode layer overlying the dielectric material (see, *e.g.*, fig. 5/step S503)
- ✓ Forming drain and source regions **104/106** on opposite sides of the gate stack (see, *e.g.*, fig. 1)

Halliyal, however, fails to show the step of inducing trapping centers in the dielectric material in response to an ionized species exposure. King (see, *e.g.*, col.14/ll.16-20), on the other hand, teaches that implanting impurity atoms into Halliyal's dielectric material layer would form a charge-trapping region within the layer. This, according to Kirkpatrick (see, *e.g.*, col.4/ll.5), would increase the number of storage sites within Halliyal's dielectric layer.

It would have been obvious at the time of the invention to one of ordinary skill in the art to induce trapping centers into the dielectric material by exposing the dielectric to an ionized species, as suggested by King and Kirkpatrick, to increase the number of storage sites within the dielectric layer.

Regarding claim 17, Halliyal shows the high-K dielectric material comprising hafnium oxide (see, *e.g.*, col.6/ll.37).

Regarding claim 20, King shows the ionized species including nitrogen (see, *e.g.*, col.3/ll.56).

Regarding claim 21, Halliyal/King/Kirkpatrick show most aspects of the instant invention (see, *e.g.*, paragraph above regarding claim 16). King (see, *e.g.*, col.6/ll.3) and Kirkpatrick (see, *e.g.*, col.4/ll.3) also teach performing the step of inducing trapping centers in the dielectric by exposing the dielectric to plasma to incorporate the trapping sites into the layer. Halliyal/King/Kirkpatrick, however, fail to specify an exposure time of about 10-100 seconds. Although they fail to specify the time of duration of the plasma exposure, performing King/Kirkpatrick's step would necessarily require a certain amount of time. The specification, on the other hand, fails to teach about the criticality

of having a specific plasma exposure time of 10-100 seconds. It has been held that time differences will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such time is critical. "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation". *In re Aller*, 220 F.2d 454,456,105 USPQ 233, 235 (CCPA 1955).

Since the applicants have not established the criticality (see next paragraph) of the exposure time claimed, it would have been obvious to one of ordinary skill in the art to use these values in the method of Halliyal/King/Kirkpatrick.

CRITICALITY

The specification contains no disclosure of either the critical nature of the claimed exposure time or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Regarding claim 22, Halliyal shows the trapping layer is deposited by an ALD method (see, *e.g.*, col.6/ll.33).

Regarding claim 25, Halliyal shows the substrate is an SOI substrate (see, *e.g.*, col.5/ll.66).

Regarding claim 26, Halliyal shows the transistor is a multi-bit transistor (see, *e.g.*, col.5/ll.20).

Regarding claim 27, Kirkpatrick uses an ion energy in the range of 10 to 300 keV and a dose in the range of about $1x10^{14}$ to $1x10^{17}$ for the step of exposing the dielectric material (see, *e.g.*, col.3/ll.56 and col.4/ll.26).

**Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Halliyal/King/Kirkpatrick in view of Chooi (US 6486080) and Agarwal (US 2001/0015453).**

Regarding claim 23, Halliyal/King/Kirkpatrick show most aspects of the instant invention (see, *e.g.*, paragraph above regarding claim 16), except for a densification anneal step after depositing the charge-trapping layer. Chooi (see, *e.g.*, col.6/ll.5-7) and Agarwal (see, *e.g.*, par.0005/ll.5-10), on the other hand, suggest following Halliyal's trapping layer deposition with an anneal step to densify the layer. This densification step would fill any oxygen vacancies developed in the layer during its formation.

It would have been obvious at the time of the invention to one of ordinary skill in the art to follow the deposition step of Halliyal/King/Kirkpatrick's trapping layer with the anneal step suggested by Chooi and Agarwal to cure oxygen vacancies developed in the layer during the deposition step.

**Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Halliyal/King/Kirkpatrick in view of Liang (US 5372957).**

Regarding claim 24, Halliyal/King/Kirkpatrick show most aspects of the instant invention (see, *e.g.*, paragraph above regarding claim 16) except for the formation of the drain and source regions comprising an angle source/drain implantation. Liang (see, *e.g.*, col.5/ll.4-7), on the other hand, teaches that angle implantation would place the ions further into the gate region of Halliyal's transistor without driving in the dopants. The resultant structure would be more immune to hot carrier degradation.

It would have been obvious at the time of the invention to one of ordinary skill in the art to form Halliyal/King/Kirkpatrick's source/drain regions using the angle implantation suggested by Liang to protect the transistor against hot carrier degradation.

**Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Halliyal/King/Kirkpatrick in view of Moslehi (US 5372957).**

Regarding claim 28, Halliyal/King/Kirkpatrick show most aspects of the instant invention (see, *e.g.*, paragraph above regarding claim 16). King (see, *e.g.*, col.6/ll.37) and Kirkpatrick (see, *e.g.*, col.4/ll.3) also teach the step of exposing the dielectric includes generating plasma. They, however, fail to show that generating the plasma includes using an inductively coupled plasma (ICP) source. Moslehi, on the other hand, suggests using an ICP source over other conventional plasma sources due to its superior process performance, throughput rate, and control capabilities including its ability to control the plasma density and ion energy independent of each other (see, *e.g.*, col.1/ll.30-64).

It would have been obvious at the time of the invention to one of ordinary skill in the art to use an ICP source to generate the plasma of Halliyal/King/Kirkpatrick, as suggested by Moslehi, because of its superior performance, throughput rate, and control capabilities.

**(10) Response to Argument**

The appellant argues:

Halliyal does not describe either an NROM or MONOS memory device, or any kind of transistor that operates on a charge-trapping or floating gate principle. More particularly, Halliyal does not describe the steps of exposing his high-k dielectric material to an ionized species, inducing charge-trapping centers in the dielectric as a result of the exposure, or a device where charge can be trapped in a gate stack.

The examiner responds:

One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In the instant case, King and Kirkpatrick were used in combination with Halliyal to demonstrate the unpatentability of the claimed invention.

Although Halliyal describes his invention as a FET transistor, he clearly specifies that his invention is not restricted to this, and may also be applied to any semiconductor device in which a high-K gate dielectric and a gate electrode are used. For example, Halliyal teaches that his invention may be used not only as a FET transistor (see, *e.g.*, Halliyal: col.5/ll.12-20), but also as a floating gate electrode memory, and as a two-bit type of memory transistor similar to the one of the instant invention (see, *e.g.*, title of the present invention).

Like Halliyal, King (see, *e.g.*, fig.20) shows a FET in which a high-K gate dielectric **1040** and a gate electrode **1060** are used. King further teaches using Halliyal's FET in a memory cell by incorporating charge traps **1030** into the high-k dielectric layer **1040** of the transistor (see, *e.g.*, King: fig.20 and col.14/ll.9-22). In this manner a memory circuit can be manufactured that would provide reduced circuit complexity, lower-power operation, and higher-speed operation (see, e.g., col.2/ll.58-65). According to Kirkpatrick (see, e.g., col.4/ll.5), King's implantation step to form a charge-trapping region within the gate dielectric would increase the number of storage sites within Halliyal/King's gate dielectric layer.

The appellant argues:

King states that a first electrically insulating layer **1020** (high-k dielectric) is formed over the substrate and that it is desirable to induce trapping centers in the insulating layer **1020** by ion implantation or diffusion (see, *e.g.*, King/col.14/ll.4-20). King further teaches that ions are selectively implanted in either the substrate, or into areas where the FETS are to be formed (see, *e.g.*, King/col.14/ll.31-51).

The examiner responds:

King also teaches a second approach, wherein the impurity atoms are directly implanted into the insulating layer **1020** to form a charge-trapping region within the insulating layer (see, *e.g.*, King/col.14/ll.45-49).

The appellant argues:

As noted in the affidavit accompanying this brief, King uses charge trapping for the purpose of inducing a negative differential resistance (NDR), and his charge-trapping centers cannot be used for non-volatile purposes. That is, King's NDR FET does not store a memory state (charge).

The examiner responds:

Whether King uses charge-trapping sites to induce an NDR effect is inconsequential to the fact that King clearly teaches a method step that increases the charge-trapping centers in a gate dielectric layer (see, *e.g.*, col.14/ll.16-26 and 45-54). It is clear to the examiner that King increases the charge-trapping centers in the dielectric to store a charge (memory state). What other purpose would a *charge-trapping center* in a dielectric have than to trap or hold a charge within the dielectric? As clearly deducted from the name itself, a charge-trapping center *will* trap a charge.

In addition to the above, in col.1/ll.18, King incorporates Tsu-Jae (US6479862) by reference. Tsu-Jae clearly teaches that the charge-trapping centers within the dielectric of King's NDR FET do store a memory state (charge). See, *e.g.*, Tsu-Jae, abstract and col.4/ll.40-62.

In response to the argument that the trapping centers in an NDR device cannot be used for *non-volatile* purposes, the recitation "a *non-volatile* memory transistor" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone, as in the present case. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

In any event, and as taught by Tsu-Jae, the trapping sites within the dielectric of King's device can exhibit anything from short/temporary storage times to very long storage times so that a useful substitute can be realized for a *non-volatile* memory structure (see, *e.g.*, Tsu-Jae, col.4/ll.65-col.5/ll.8).

As an endnote to this response, Tsu-Jae is a teaching reference that King incorporated by reference. It is used herein to illustrate that the charge-trapping centers in King do hold a charge or memory state, and it should not be construed as changing the previous grounds of rejection.

The appellant argues:

Kirkpatrick discloses an ion implantation process for forming charge-trapping sites into an insulator material. Unlike the claimed invention, which recites forming charge-trapping centers in a high-K dielectric, Kirkpatrick discloses a silicon dioxide insulator. Unlike the claimed invention, which recites a transistor memory device, Kirkpatrick discloses a diode memory.

The examiner responds:

One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In the instant case, Kirkpatrick was used in combination with Halliyal and King to demonstrate the unpatentability of the claimed invention.

Halliyal, for example, describes his invention as a FET transistor and he clearly specifies that his invention may also be applied to any semiconductor device in which a high-K gate dielectric and a gate electrode are used. For example, Halliyal teaches that his invention may be used not only as a FET transistor, but also as a memory transistor (see, *e.g.*, Halliyal: col.5/ll.12-20).

Like Halliyal, King (see, *e.g.*, fig.20) shows a FET in which a high-K gate dielectric **1040** and a gate electrode **1060** are used. King further teaches incorporating charge traps **1030** in the high-K dielectric layer **1040** of Halliyal's FET (see, *e.g.*, King: fig.20 and col.14/ll.9-22). In this manner a memory circuit can be manufactured that would provide reduced circuit complexity, lower-power operation, and higher-speed operation (see, *e.g.*, col.2/ll.58-65). According to Kirkpatrick (see, *e.g.*, col.4/ll.5), King's implantation step to form a charge-trapping region within the gate dielectric would increase the number of storage sites within Halliyal/King's high-K gate dielectric layer.

The appellant argues:

Kirkpatrick is the only reference that mentions a memory application.

The examiner responds:

Halliyal teaches that his invention may be used not only as a FET transistor (see, *e.g.*, Halliyal: col.5/ll.12-20), but also as memory transistor. In addition, King also clearly mentions a memory application (see, *e.g.*, col.1/ll.53-57).

The appellant argues:

No evidence has been provided in the Office action that an expert in the art would be motivated to modify a process that protects a high-k dielectric from reduction (Halliyal), in light of an NDR FET or a memory diode, to increase the number of storage sites in a dielectric layer. On its face this assertion is flawed because Halliyal discloses no storage site in the first place. It is not logical to base the rejection of the applicant's memory transistor upon a primary reference that is not itself a memory device.

The examiner responds:

Although Halliyal describes his invention as a FET transistor, he clearly specifies that his invention is not restricted to this, and may also be applied to any semiconductor device in which a high-K gate dielectric and a gate electrode are used, for example, memory devices (see, *e.g.*, col.5/ll.18-20). In fact, Halliyal specifically says that his invention may be applied to a two-bit type of memory device similar to the one of the instant invention (see, *e.g.*, col.5/ll.20-24). Halliyal shows all claimed method steps except for inducing trapping centers by exposing the dielectric material to an ionized species.

King teaches that devices exhibiting NDR characteristics have long been sought after in the history of semiconductor devices (see, *e.g.*, King; col.1/ll.60-63 and col.2/ll.1-5). Faster and more efficient circuits may be implemented using these NDR devices (see, *e.g.*, King: col.2/ll.58-65). To form an NDR device, King teaches ion implanting Halliyal's gate dielectric to incorporate trapping centers into the dielectric. These trapping centers are incorporated into the dielectric by subjecting it to the ionized species involved in every ion implantation step (see, *e.g.*, King: col.5/ll.48-55 and

col.6/ll.36-40). Accordingly, one of ordinary skill in the art would have found it obvious to induce NDR characteristics into Halliyal's FET by incorporating trapping sites into the dielectric, as suggested by King, so that the FET device may be implemented into faster and more efficient circuits.

The appellant argues:

The examiner states that it would have been obvious to combine the teachings of King and Kirkpatrick with Halliyal to increase the number of storage sites within the dielectric layer. This statement is insufficient to support a *prima facie* case of obviousness.

The examiner responds:

One of ordinary skill in the art would have understood the advantages associated to increasing the number of storage sites within a dielectric layer. Kirkpatrick, for example, teaches that the density of defects, or trapping sites, directly affects the number of charges storable in the dielectric (see, *e.g.*, col.1/ll.48-52). The more trapping sites within the dielectric, the higher the number of charges that can be stored in the dielectric. One skilled in the art would also have known that providing additional trapping sites within the dielectric would reduce variations in the reading and writing behavior of the device (see, *e.g.*, Kirkpatrick: col.1/ll.60-66). Accordingly, increasing the number of storage sites within the dielectric is sufficient motivation to support a *prima facie* case of obviousness.

The appellants argue:

Even if an expert were given the three references as a foundation, there is no reasonable expectation that this expert could derive the claimed invention, since none of the references suggest the claimed gate stack structure. That is, none of the references discloses a memory transistor with a charge-trapping region formed from a single layer of high-K dielectric (without an underlying or overlying oxide layer).

The examiner responds:

King clearly shows the above features of the claimed invention. See, *e.g.*, fig. 20 where King shows a charge-trapping region **1030** formed from a single layer **1020** of high-K dielectric material (without an underlying or overlying *oxide* layer). Please note that although King shows layer **1040** overlying the high-K dielectric material, this layer can consist entirely of $Si_3N_4$, which is not an *oxide* layer (see, *e.g.*, King: col.15/ll.4). Accordingly, King clearly shows (see, *e.g.*, fig.20) the claimed steps of: depositing a single layer of high-K dielectric material **1030**, without an underlying or overlying *oxide* insulator layer; exposing the high-K dielectric material to an ionized species (see, *e.g.*, col.14/ll.45-54); and, in response to the ionized species exposure, inducing trapping centers **1030** into the high-K dielectric material **1020** (see, *e.g.*, col.1/4ll.45-54).

The appellants argue:

Chooi describes the densification of a metal oxide. Agarwal describes densification to cure oxygen vacancies in a high-K dielectric. It is not clear how these references have any application to the claimed invention, which performs a densification annealing to prevent delamination of the gate (see, *e.g.*, pp.12/ll.25-25).

The examiner responds:

The fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

The appellant argues:

Even if Liang describes an angle implantation to form source/drain region, it is not apparent that Liang suggests any modification to the ion implantation processes of either King or Kirkpatrick, or to Halliyal's high-K dielectric reduction protection process.

The examiner responds:

As noted by the appellant, the angled implantation recited in claim 24 is used to form source and drain regions. The implantation steps of King and Kirkpatrick are different to those of Liang. The teachings of Liang were not used to modify the implantation steps of King and Kirkpatrick. Liang was used to teach that angled implantation could be used to form source/drain regions that would protect a transistor against hot carrier degradation; whereas King and Kirkpatrick were used to teach that ion implantation could be used to generate storage sites within a dielectric layer. See, *e.g.*, Liang: col.5/ll.4-7; King: col.6/ll.36-40; and Kirkpatrick: col.3/ll.42-60.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

An appeal conference was held on 1/30/2007 between Mr. Marcos D. Pizarro (Primary Examiner), Mr. Ricky Mack (Supervisory Patent Examiner), and Mr. Carl Whitehead (Supervisory Patent Examiner) as the conferees.

Respectfully submitted,

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